Claims

What is claimed is:

1. An overetch system comprising:
a metal etcher for performing overetching;
a target device placed in the metal etcher;
an overetch controller coupled the metal etcher, to control overetching and to control removal of an overetch amount of material from the target device.

2. The overetch system of claim 1, wherein the target device is a wafer having at least one semiconductor device having a metal layer comprised of a material selected from the group comprising aluminum and aluminum alloy.

3. The overetch system of claim 2, wherein the wafer has an oxide layer covered with remaining residue from a metal etch process.

4. The overetch system of claim 3, wherein the remaining residue comprises unremoved aluminum.

5. The overetch system of claim 1, wherein the metal etcher is able to perform metal etching and metal overetching.

6. The overetch system of claim 1, wherein the overetch controller controls overetching utilizing feedback data.

7. The overetch system of claim 1, further comprising at least one sensor to measure feedback data of the target device during overetching and to provide the feedback data to the overetch controller, wherein the overetch controller utilizes the feedback data to control overetching.

8. The overetch system of claim 1, further comprising a device model to provide overetch parameters to the overetch controller.

9. The overetch system of claim 1, wherein the overetch controller comprises:
an overetch time controller;
a set of etch control models; and
a control system.

10. The overetch system of claim 9, wherein the overetch time controller initiates and halts the metal etcher during overetch processes.

11. The overetch system of claim 10, wherein the set of etch control models include layout data, etchable area and percentage of etchable area.

12. The overetch system of claim 9, wherein the control system is implemented on a computer system.

13. The overetch system of claim 9, wherein the control system identifies the target device and selects at least one relevant model form the set of etch control models.

14. The overetch system of claim 9, wherein the set of etch control models comprise two dimensional information.

15. The overetch system of claim 9, wherein the set of etch control models comprise three dimensional information.

16. An overetch system comprising:
a target device;
a metal etching means for removing an overetch amount of material from the target device;

an overetch control means for controlling the metal etching means, the overetch control means comprising:

a set of etch control models;

a timer means for initiating and halting the metal etching means; and

a control means for selecting at least one relevant model from the set of etch control models and determining an overetch endpoint.

17. A method of fabricating a semiconductor device comprising:

providing a wafer having at least one semiconductor layer;

forming an oxide layer over the at least one semiconductor layer;

forming a plurality of trenches in the oxide layer;

forming a metal layer over the oxide layer and in the plurality of trenches;

depositing a resist layer over the metal layer;

using a mask and developing selected portions of the resist layer;

removing the selected portions of the resist layer;

performing a metal etch to substantially remove the metal layer leaving remaining residue and metal lines in the plurality of trenches;

determining at least one overetch parameter utilizing an etch rate model; and

performing an overetch according to the at least one overetch parameter to remove a tolerable amount of the oxide layer and the remaining residue.

18. The method of claim 17, the at least one overetch parameter comprising an overetch rate, overetch time, profile, and uniformity.

19. The method of claim 17, further comprising:

measuring the wafer while performing the overetch for compliance with the at least one overetch parameter; and

modifying the overetch process on non-compliance with the at least one overetch parameter.

20. The method of claim 17 further comprising forming a barrier layer in the plurality of trenches.

21. A method of fabricating a semiconductor device comprising:

providing a semiconductor device having remaining residue on a first layer, the semiconductor device having a layout of a circuit design;

utilizing a device model to determine overetch parameters, the device model corresponding to the layout of the semiconductor device; and

performing an overetch according to the overetch parameters while monitoring the semiconductor device for compliance with the overetch parameters to remove a tolerable amount of the first layer and the remaining residue.

22. The method of claim 21, wherein the overetch parameters comprise an overetch endpoint determined as a function of etchable area and etch rate regions of the device model.

23. A method of fabricating an overetch control model, the method comprising:

designing a circuit;

determining a layout for the circuit based on desired functionality;

modifying the layout according to design rules;

modifying the layout to reduce adverse effects;

determining an etchable area;

determining at least one etch rate region;

assigning an etch rate to the at least one etch rate region;

calculating an acceptable overall etch rate;

simulating an overetch on the overetch control model according to overetch parameters; and

on results of the overetch being unacceptable, modifying the overetch control model as necessary.

24. The method of claim 23, wherein calculating an acceptable overall etch rate comprises calculating an etch rate to sufficiently remove remaining residue and a tolerable amount of oxide from the semiconductor devices.

25. The method of claim 23, further comprising performing an overetch process on a semiconductor device utilizing the overetch control model.